FIG. 1

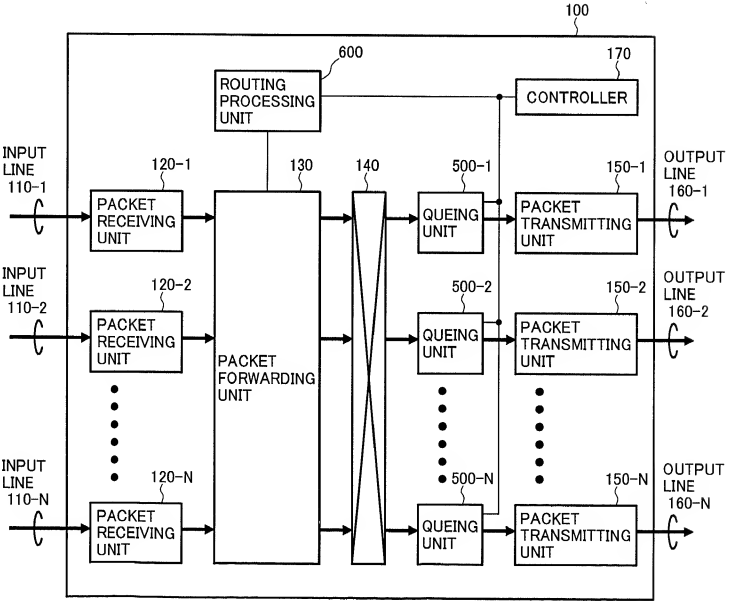

100
600
ROUTING PROCESSING UNIT
170
CONTROLLER
INPUT LINE 110-1
120-1
PACKET RECEIVING UNIT
130
PACKET FORWARDING UNIT
140
500-1
QUEING UNIT
150-1
PACKET TRANSMITTING UNIT
OUTPUT LINE 160-1
INPUT LINE 110-2
120-2
PACKET RECEIVING UNIT
500-2
QUEING UNIT
150-2
PACKET TRANSMITTING UNIT
OUTPUT LINE 160-2
INPUT LINE 110-N
120-N
PACKET RECEIVING UNIT
500-N
QUEING UNIT
150-N
PACKET TRANSMITTING UNIT
OUTPUT LINE 160-N

FIG. 2

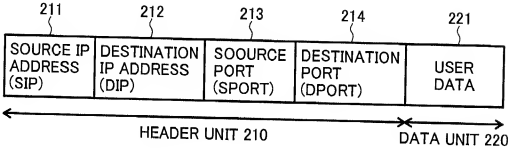

211
212
213
214
221
SOURCE IP ADDRESS (SIP)
DESTINATION IP ADDRESS (DIP)
SOOURCE PORT (SPORT)
DESTINATION PORT (DPORT)
USER DATA
HEADER UNIT 210
DATA UNIT 220

FIG. 3

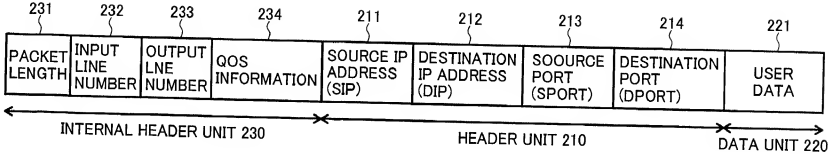

231
232
233
234
211
212
213
214
221
PACKET LENGTH
INPUT LINE NUMBER
OUTPUT LNE NUMBER
QOS INFORMATION
SOURCE IP ADDRESS (SIP)
DESTINATION IP ADDRESS (DIP)
SOOURCE PORT (SPORT)
DESTINATION PORT (DPORT)
USER DATA
INTERNAL HEADER UNIT 230
HEADER UNIT 210
DATA UNIT 220

FIG. 4

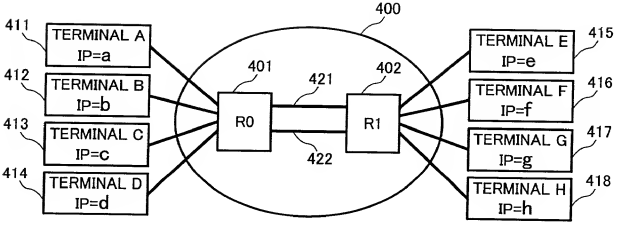

400
411
TERMINAL A
IP=a
412
TERMINAL B
IP=b
413
TERMINAL C
IP=c
414
TERMINAL D
IP=d
401
R0
421
422
402
R1
TERMINAL E
IP=e
415
TERMINAL F
IP=f
416
TERMINAL G
IP=g
417
TERMINAL H
IP=h
418

FIG. 5

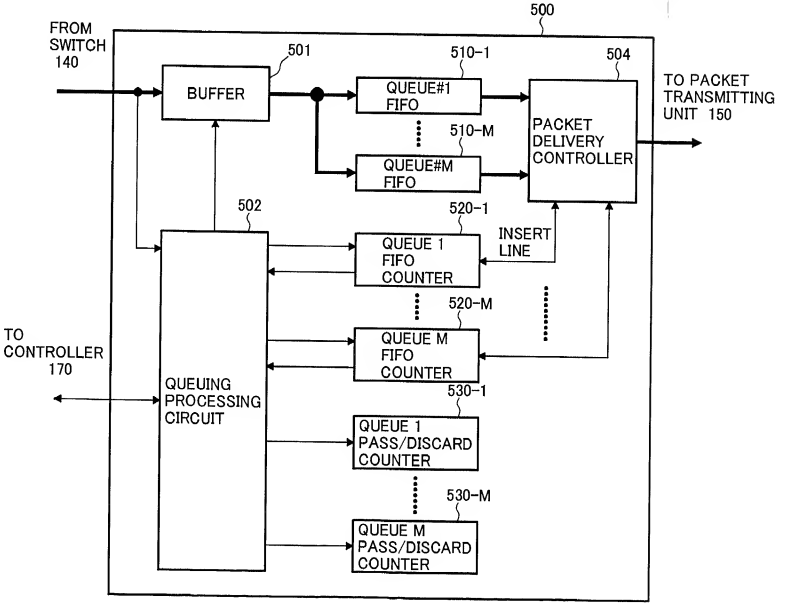

500
FROM SWITCH 140
501
510-1
504
BUFFER
QUEUE#1 FIFO
TO PACKET TRANSMITTING UNIT 150
510-M
PACKET DELIVERY CONTROLLER
QUEUE#M FIFO
502
520-1
INSERT LINE
QUEUE 1 FIFO COUNTER
520-M
TO CONTROLLER 170
QUEUE M FIFO COUNTER
530-1
QUEUING PROCESSING CIRCUIT
QUEUE 1 PASS/DISCARD COUNTER
530-M
QUEUE M PASS/DISCARD COUNTER

FIG. 6

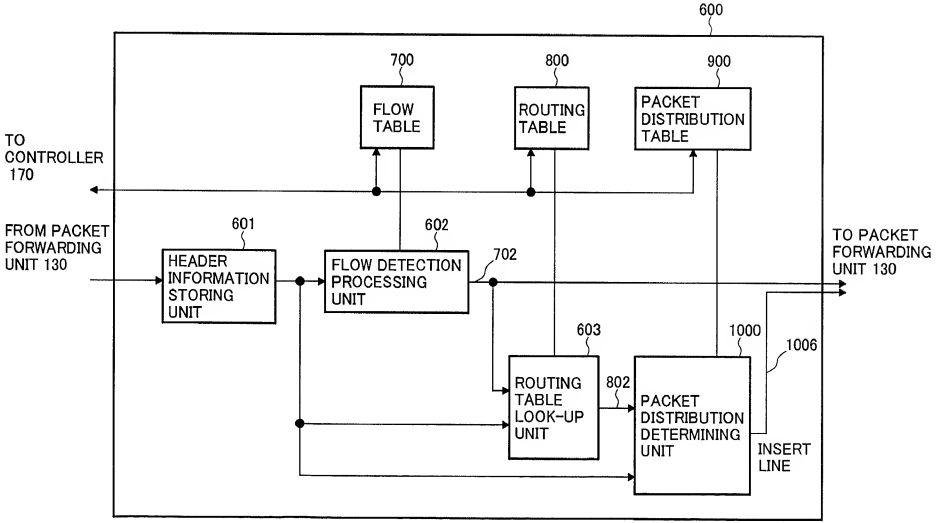

600
700
800
900
FLOW TABLE
ROUTING TABLE
PACKET DISTRIBUTION TABLE
TO CONTROLLER 170
FROM PACKET FORWARDING UNIT 130
601
602
HEADER INFORMATION STORING UNIT
FLOW DETECTION PROCESSING UNIT
702
TO PACKET FORWARDING UNIT 130
603
1000
1006
ROUTING TABLE LOOK-UP UNIT
802
PACKET DISTRIBUTION DETERMINING UNIT
INSERT LINE

FIG. 7

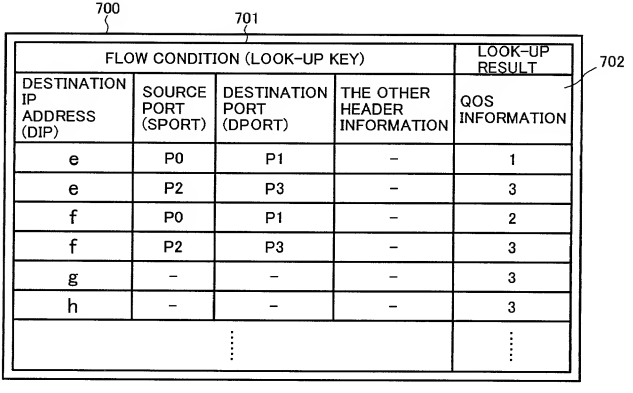

700
701
FLOW CONDITION (LOOK-UP KEY)
LOOK-UP RESULT
702
DESTINATION IP ADDRESS (DIP)
SOURCE PORT (SPORT)
DESTINATION PORT (DPORT)
THE OTHER HEADER INFORMATION
QOS INFORMATION
e P0 P1 – 1
e P2 P3 – 3
f P0 P1 – 2
f P2 P3 – 3
g – – – 3
h – – – 3

FIG. 8

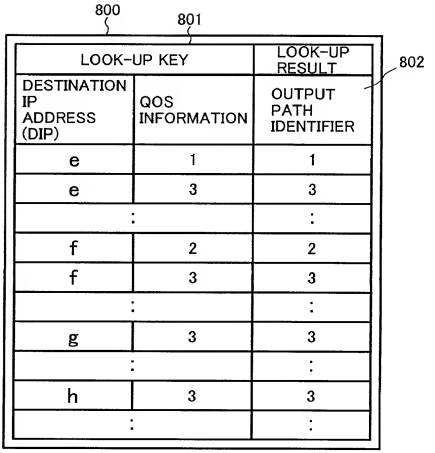

800
801
802
LOOK-UP KEY
LOOK-UP RESULT
DESTINATION IP ADDRESS (DIP)
QOS INFORMATION
OUTPUT PATH IDENTIFIER
e 1 1
e 3 3
f 2 2
f 3 3
g 3 3
h 3 3

FIG. 9

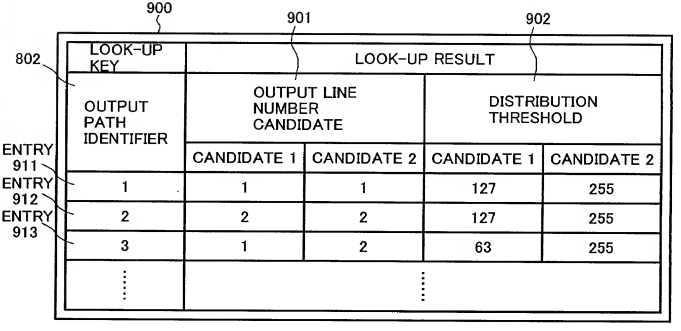
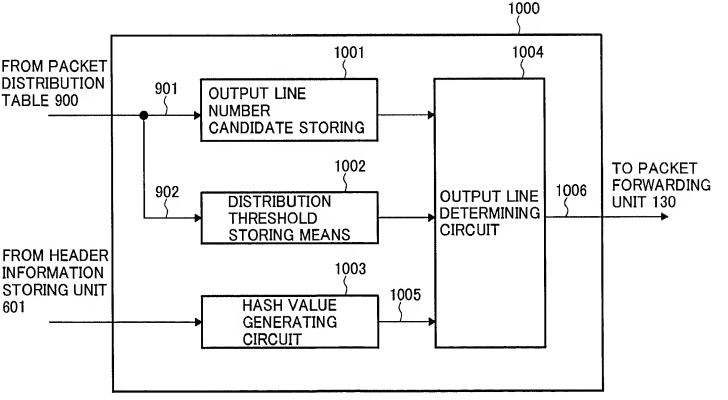

900
901
902
802
LOOK-UP KEY
LOOK-UP RESULT
OUTPUT PATH IDENTIFIER
OUTPUT LINE NUMBER CANDIDATE
DISTRIBUTION THRESHOLD
CANDIDATE 1
CANDIDATE 2
CANDIDATE 1
CANDIDATE 2
ENTRY 911
ENTRY 912
ENTRY 913
1
1
1
127
255
2
2
2
127
255
3
1
2
63
255

FIG. 10


1000
1001
1004
FROM PACKET DISTRIBUTION TABLE 900
901
OUTPUT LINE NUMBER CANDIDATE STORING
1002
902
DISTRIBUTION THRESHOLD STORING MEANS
OUTPUT LINE DETERMINING CIRCUIT
1006
TO PACKET FORWARDING UNIT 130
FROM HEADER INFORMATION STORING UNIT 601
1003
1005
HASH VALUE GENERATING CIRCUIT

INTEL 3462.1601

FIG. 11

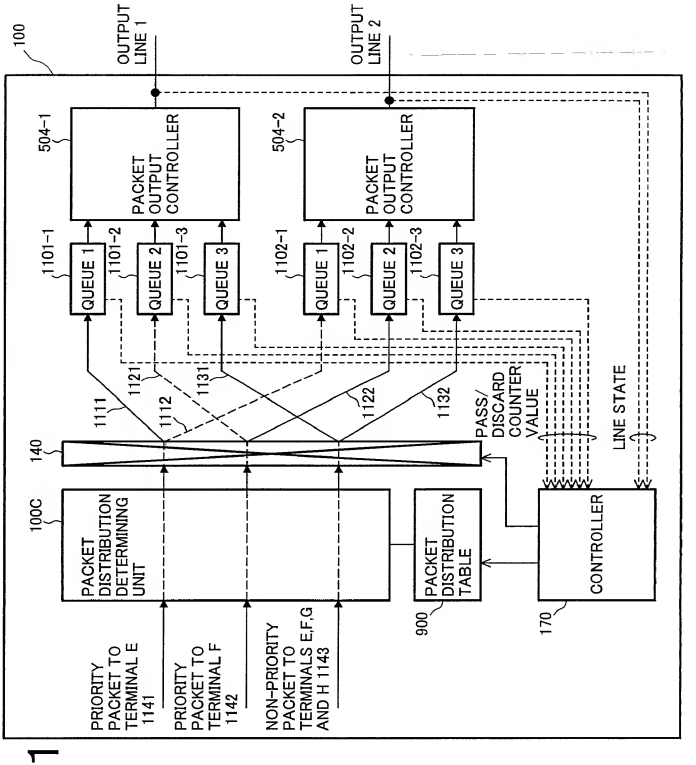
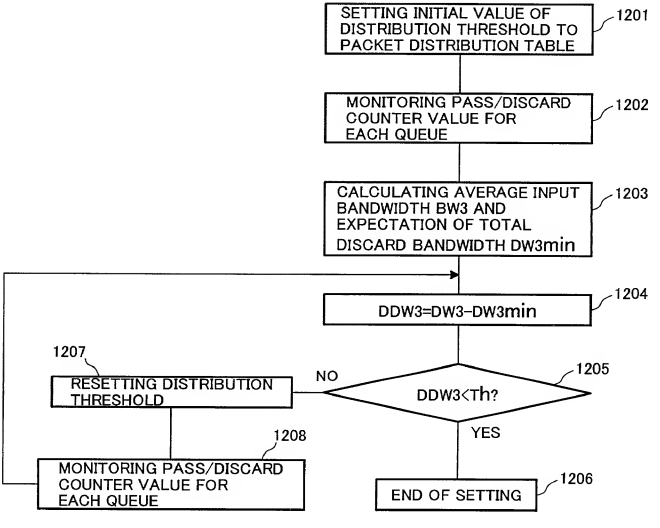


FIG. 12


SETTING INITIAL VALUE OF DISTRIBUTION THRESHOLD TO PACKET DISTRIBUTION TABLE
1201
MONITORING PASS/DISCARD COUNTER VALUE FOR EACH QUEUE
1202
CALCULATING AVERAGE INPUT BANDWIDTH BW3 AND EXPECTATION OF TOTAL DISCARD BANDWIDTH DW3min
1203
DDW3=DW3−DW3min
1204
DDW3<Th?
1205
NO
YES
RESETTING DISTRIBUTION THRESHOLD
1207
MONITORING PASS/DISCARD COUNTER VALUE FOR EACH QUEUE
1208
END OF SETTING
1206